WHAT IS CLAIMED IS

1. A digital sampling instrument for the multichannel Nth order interpolative playback of digital audio data output samples stored in a waveform memory comprising:

coefficient logic means for generating N coefficients for each channel for each of said output samples,

cache memory means for storing at least N waveform memory samples for each channel,

convolution means for computing a sum of N products of the contents of said cache memory means times said coefficients for each of several ones of said output channels, and

means for outputting said sum of products for each of said channels.

2. An instrument as in claim 1 wherein said cache memory is a dual port memory.

3. An instrument as in claim 1 wherein said cache memory is comprises two single port memories.

4. An instrument as in claim 1 wherein said cache memory is of size N samples per channel.

5. An instrument as in claim 1 wherein said cache memory is of size N+1 samples per channel.

6. An instrument as in claim 1 also including a priority circuit for determining which channel's current address is used to load said cache memory.

7. An instrument as in claim 6 wherein said priority circuit includes two levels of priority for each channel.

8. An instrument as in claim 1 also including an address register file containing the integer part of a current address for each channel, and the required cache update size for each channel.

9. An instrument as in claim 8 wherein said address register file is responsive to an address update unit which increments said current address, and also responsive to a memory access unit which address the waveform memory at said integer part current address.

10. An instrument as in claim 8 including a cache base address stored in said address register file.

11. An instrument in claim 1 wherein said waveform memory includes a plurality of different memory types.

12. A digital sampling instrument for the multichannel Nth order interpolative playback of digital audio data stored in a waveform memory operating during waveform memory cycles comprising:

a plurality of interpolator circuits utilizing a single waveform memory, and

bus request and bus acknowledge signals shared among said plurality of interpolator circuits for determining whether a single bus has control of the waveform memory at any given waveform memory cycle.

13. In instrument as in claim 12 in which each of said interpolator circuits including:

coefficient logic means for generating N coefficients for each channel for each output sample,

cache memory means for storing at least N waveform memory samples for each channel,

convolution means for computing a sum of N products of the contents of said cache memory times said coefficients for each of several output channels, and

means for outputting said sum of products for each of said channels.